CLAIMS

1. A retention device for a dynamic logic stage having an output inverter, said retention device being for stabilizing the respective first and second logic output levels of said logic stage, said inverter being connected to provide an inversion of said logic output for use by said retention device as a feedback signal for performing said stabilizing, said retention device comprising:

a switching element comprising a first and a second active elements connected in series;

a control input for receiving a delayed clock signal; and

a feedback input for receiving said inverted logic signal;

therewith to switch between a first and a second retention states in accordance with said feedback and delayed clock signals, said first and second retention states being respectively for stabilizing said first and a second logic output levels.

2. A retention device for a dynamic logic stage according to claim 1, configured to prevent said logic output from discharging from said first logic output level to said second logic output level when in said first retention state.

3. A retention device for a dynamic logic stage according to claim 2, wherein said configuring to prevent comprises providing said first logic output level at an output of said retention device.

4. A retention device for a dynamic logic stage according to claim 1, configured to enable said logic output to discharge from said first logic output level to said second logic output level when in said second retention state.

5. A retention device for a dynamic logic stage according to claim 4, wherein said configuring to enable comprises providing a high impedance at an output of said retention device.

6. A retention device for a dynamic logic stage according to claim 1, wherein said output inverter is further connected to provide a buffered inverted logic signal to a second dynamic logic stage.

7. A retention device for a dynamic logic stage according to claim 1, wherein said first active element is configured to be switched by said delayed clock signal.

8. A retention device for a dynamic logic stage according to claim 1, wherein said second active element is configured to be switched by said feedback signal.

9. A retention device for a dynamic logic stage according to claim 1, further comprising a clock delayer connected between a dynamic logic stage clock input and said control input.

10. A retention device for a dynamic logic stage according to claim 9, wherein said clock delayer comprises an inverter.

11. A retention device for a dynamic logic stage according to claim 9, wherein said clock delayer comprises a chain of inverters.

12. A retention device for a dynamic logic stage according to claim 9, wherein said clock delayer comprises at least one transmission gate.

13. A retention device for a dynamic logic stage according to claim 9, wherein said clock delayer comprises at least one wire delay line.

14. A retention device for a dynamic logic stage according to claim 1, wherein said active elements comprise transistors.

15. A retention device for a dynamic logic stage according to claim 1, wherein said active elements comprise field effect transistors (FETs).

16. A retention device for a dynamic logic stage according to claim 1, wherein said active elements comprise p-type metal oxide semiconductor (PMOS) field effect transistors.

17. A retention device for a dynamic logic stage, said retention device being for stabilizing the respective first and second logic output levels of said logic stage, said retention device comprising:

a switching element comprising a first and a second active elements connected in series;

a control input for receiving a delayed clock signal; and

a feedback input for receiving a feedback signal comprising a logic output signal of said dynamic logic stage;

therewith to switch between a first and a second retention states in accordance with said feedback and delayed clock signals, said first and second retention states being respectively for stabilizing said first and a second logic output levels.

18. A retention device for a dynamic logic stage according to claim 17, configured to prevent said logic output from discharging from said first logic output level to said second logic output level when in said first retention state.

19. A retention device for a dynamic logic stage according to claim 18, wherein said configuring to prevent comprises providing said first logic output level at an output of said retention device.

20. A retention device for a dynamic logic stage according to claim 17, configured to enable said logic output to discharge from said first logic output level to said second logic output level when in said second retention state.

21. A retention device for a dynamic logic stage according to claim 20, wherein said configuring to enable comprises providing a high impedance at an output of said retention device.

22. A stabilized dynamic logic stage, comprising:

a pull-up element, for switching said stabilized dynamic logic stage between a precharge phase and an evaluate phase in accordance with an input clock signal;

a logic network associated with said pull-up element, for providing at a logic output an output logic signal comprising a result of a predefined logic operation performed upon input logic signals;

an inverter associated with said logic output, for generating a feedback signal as an inverse of said output logic signal; and

a retention device associated with said pull-up element, said inverter, and said logic network, said retention device being for stabilizing the respective first and second logic output levels of said logic stage, said retention device comprising:

a switching element comprising a first and a second active elements connected in series;

a control input for receiving a delayed version of said input clock signal; and

a feedback input for receiving said inverted logic signal;

therewith to switch between a first and a second retention states in accordance with said feedback and delayed clock signals, said first and second retention states being respectively for stabilizing said first and a second logic output levels.

23. A stabilized dynamic logic stage according to claim 22, configured to prevent said logic output from discharging from said first logic output level to said second logic output level when in said first retention state.

24. A stabilized dynamic logic stage according to claim 23, wherein said configuring to prevent comprises providing said first logic output level at an output of said retention device.

25. A stabilized dynamic logic stage according to claim 22, configured to enable said logic output to discharge from said first logic output level to said second logic output level when in said second retention state.

26. A stabilized dynamic logic stage according to claim 25, wherein said configuring to enable comprises providing a high impedance at an output of said retention device.

27. A stabilized dynamic logic stage according to claim 22, wherein said pull-up element comprises a transistor.

28. A stabilized dynamic logic stage according to claim 22, wherein said pull-up element comprises an FET.

29. A stabilized dynamic logic stage according to claim 22, wherein said pull-up element comprises a PMOS field effect transistor.

30. A stabilized dynamic logic stage according to claim 22, wherein said logic network comprises a network of transistors.

31. A stabilized dynamic logic stage according to claim 22, wherein said logic network comprises a network of FETs.

32. A stabilized dynamic logic stage according to claim 22, wherein said logic network comprises a network of NMOS field effect transistors.

33. A stabilized dynamic logic stage according to claim 22, wherein said first active element is configured to be switched by said delayed clock signal.

34. A stabilized dynamic logic stage according to claim 22, wherein said second active element is configured to be switched by said feedback signal.

35. A stabilized dynamic logic stage according to claim 22, further comprising a clock delayer connected between a dynamic logic stage clock input and said control input.

36. A stabilized dynamic logic stage according to claim 35, wherein said clock delayer comprises an inverter.

37. A stabilized dynamic logic stage according to claim 35, wherein said clock delayer comprises at least one of a group of delay elements comprising: an inverter, a transmission gate, and a wire delay line.

38. A stabilized dynamic logic stage according to claim 22, wherein said active elements comprise transistors.

39. A stabilized dynamic logic stage according to claim 22, wherein said active elements comprise field effect transistors (FETs).

40. A stabilized dynamic logic stage according to claim 22, wherein said active elements comprise p-type metal oxide semiconductor (PMOS) field effect transistors.

41. A method for providing a stabilized dynamic logic stage comprising:
providing a pull-up element, having a clock input for receiving a clock signal, and a pull-up output;

connecting a logic output of a logic network to said pull-up output, said logic network having a plurality of logic inputs;

connecting an inverter to said logic output and said pull-up element, such that an input of said inverter is connected to said logic output;

forming a switching element by connecting a first and a second active elements in series;

connecting said switching element between said inverter and said logic network, such that a retention output of said switching element is connected to said logic output, and a feedback input of said switching element is connected to an output of said inverter; and

connecting a control input of said switching element to receive a delayed version of said clock signal.

42. A method for providing a stabilized dynamic logic stage according to claim 41, further comprising connecting a delay stage to said clock signal to provide said delayed version of said clock signal.

43. A method for providing a stabilized dynamic logic stage according to claim 42, wherein said delay stage comprises an inverter.

44. A method for providing a stabilized dynamic logic stage according to claim 42, wherein said delay stage comprises a chain of inverters.

45. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said active elements comprise transistors.

46. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said active elements comprise field effect transistors (FETs).

47. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said active elements comprise p-type metal oxide semiconductor (PMOS) field effect transistors.

48. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said pull-up element comprises a transistor.

49. A method for providing a stabilized dynamic logic stage according to claim 48, wherein said pull-up element comprises a FET.

50. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said pull-up element comprises a PMOS field effect transistor.

51. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said logic network comprises a network of transistors.

52. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said logic network comprises a network of FETs.

53. A method for providing a stabilized dynamic logic stage according to claim 41, wherein said logic network comprises a network of NMOS field effect transistors.